The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-78. (Canceled)

78. (Currently Amended) A semiconductor device comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively, wherein said channel region comprises semi-amorphous silicon;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary in said semiconductor layer, said region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more,

wherein one boundary of said region is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

79. (Previously Presented) A device according to claim 78 wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

80.-81. (Canceled)

82. (Previously Presented) A device according to claim 78 wherein said semiconductor layer comprises amorphous silicon.

83. (Currently Amended) A device according to [[clam]] claim 78 wherein a concentration of said element in said channel region is lower than that of said element in said region.

84. (Currently Amended) A semiconductor device comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively, wherein said channel region comprises semi-amorphous silicon;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region having a higher energy band gap than any of said source, drain, and channel regions,

wherein said region is formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary, and one boundary of said region is located within the channel region and is not aligned with edges of the gate electrode.

85. (Previously Presented) A device according to claim 84 wherein said semiconductor device has transistors selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

86.-87. (Canceled)

88. (Previously Presented) A device according to claim 84 wherein said semiconductor layer comprises amorphous silicon.

89. (Currently Amended) A device according to [[clam]] claim 84 wherein said region includes one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more.

90. (Currently Amended) A semiconductor device comprising:

a pixel portion formed over [[an]] a substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively, wherein said channel region comprises semi-amorphous silicon;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region formed in said semiconductor layer, said region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more,

wherein said region is formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary, and one boundary of said region is located within the channel region and is not aligned with edges of the gate electrode.

91. (Previously Presented) A device according to claim 90 wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

92.-93. (Canceled)

94. (Previously Presented) A device according to claim 90 wherein said driver circuit has at least a CMOS circuit comprising a pair of an n-channel TFT and a p-channel TFT.

95. (Currently Amended) A device according to [[clam]] claim 90 wherein a concentration of said element in said channel region is lower than that of said element in said region.

96. (Currently Amended) A semiconductor device comprising:

a pixel portion formed over [[an]] a substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively, wherein said channel region comprises semi-amorphous silicon;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region having a higher energy band gap than any of said source, drain, and channel regions,

wherein said region is formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary, and one boundary of said region is located within the channel region and is not aligned with edges of the gate electrode.

97. (Previously Presented) A device according to claim 96 wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

98.-99. (Canceled)

100. (Previously Presented) A device according to claim 96 wherein said driver circuit has at least a CMOS circuit comprising a pair of an n-channel TFT and a p-channel TFT.

101. (Currently Amended) A device according to [[clam]] claim 96 wherein said region ~~containing~~ contains one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more.

102. (Currently Amended) A semiconductor device comprising:

a pixel portion formed over [[an]] a substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween, wherein said channel region comprises semi-amorphous silicon; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including carbon and overlapping both a portion of said channel region and a portion of said source and drain regions at a concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including carbon is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

103. (Previously Presented) A device according to claim 102 wherein said semiconductor layer comprises amorphous silicon.

104. (Previously Presented) A device according to claim 102 wherein said driver circuit has at least a CMOS circuit comprising a pair of an n-channel TFT and a p-channel TFT.

105. (Previously Presented) A device according to claim 102 wherein said channel region contains boron at a concentration of from 1×10^{15} to 5×10^{17} atoms/cm^3.

106.-107. (Canceled)

108. (Currently Amended) A device according to claim 104 wherein an absolute value of a threshold voltage of said n-channel TFT is approximately equivalent to that of said p-channel TFT.

109. (Previously Presented) A device according to claim 102 wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

110. (Currently Amended) A semiconductor device comprising:

a pixel portion formed over [[an]] a substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween, wherein said channel region comprises semi-amorphous silicon; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including nitrogen and overlapping both a portion of said channel region and a portion of said source and drain regions at a concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including nitrogen is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

111. (Previously Presented) A device according to claim 110 wherein said channel region contains boron at a concentration of from 1×10^{15} to 5×10^{17} atoms/cm^3.

112. (Previously Presented) A device according to claim 110 wherein said driver circuit has at least a CMOS circuit comprising a pair of an n-channel TFT and a p-channel TFT.

113. (Previously Presented) A device according to claim 110 wherein said semiconductor layer comprises crystalline silicon.

114.-115. (Canceled)

116. (Currently Amended) A device according to claim 112 wherein an absolute value of a threshold voltage of said n-channel TFT is approximately equivalent to that of said p-channel [[TFTs]] TFT.

117. (Previously Presented) A device according to claim 110 wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of a stagger type, inverted stagger type, planar type, and inverted planar type transistors.

118. (Currently Amended) A semiconductor device comprising:

a pixel portion formed over [[an]] a substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween, wherein said channel region comprises semi-amorphous silicon; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including oxygen and overlapping both a portion of said channel region and a portion of said source and drain regions at a concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including oxygen is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

119. (Previously Presented) A device according to claim 118 wherein said channel region contains boron at a concentration of from 1×10^{15} to 5×10^{17} atoms/cm^3.

120. (Previously Presented) A device according to claim 118 wherein said driver circuit has at least a CMOS circuit comprising a pair of an n-channel TFT and a p-channel TFT.

121. (Previously Presented) A device according to claim 118 wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

122.-123. (Canceled)

124. (Previously Presented) A device according to claim 118 wherein said semiconductor layer comprises amorphous silicon.

125. (Previously Presented) A device according to claim 118 wherein a concentration of said element in said channel region is lower than that of said element in said region.

126. (Currently Amended) A semiconductor device comprising:

a pixel portion formed over [[an]] a substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween, wherein said channel region comprises semi-amorphous silicon;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region formed in the vicinity of at least one of a source-channel boundary and a drain-channel boundary in said semiconductor layer, said region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more,

wherein one boundary of said region is located within said channel region and is not aligned with edges of the gate electrode.

127. (Previously Presented) A device according to claim 126 wherein said channel region contains boron at a concentration of from 1×10^{15} to 5×10^{17} atoms/cm^3.

128. (Previously Presented) A device according to claim 126 further comprising:

a first interlayer insulating film over said semiconductor layer and said gate electrode, said first interlayer insulating film comprising inorganic material;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising organic resin; and

a pixel electrode on said second interlayer insulating film.

129. (Previously Presented) A device according to claim 126 wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

130.-131. (Canceled)

132. (Previously Presented) A device according to claim 126 wherein said semiconductor layer comprises amorphous silicon.

133. (Previously Presented) A device according to claim 126 wherein a concentration of said element in said channel region is lower than that of said element in said region.

134. (Currently Amended) A semiconductor device comprising:

a pixel portion formed over [[an]] a substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween, wherein said channel region comprises semi-amorphous silicon;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region having a higher energy band gap than any of said source, drain, and channel regions, said region formed in the vicinity of at least one of a source-channel boundary and a drain-channel boundary in the semiconductor layer,

wherein one boundary of said region is located within said channel region and is not aligned with edges of the gate electrode.

135. (Previously Presented) A device according to claim 134 wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

136.-137. (Canceled)

138. (Previously Presented) A device according to claim 134 wherein said gate electrode comprises one selected from the group consisting of a silicon film containing phosphorus, a multilayer film comprising silicon and molybdenum, and a multilayer film comprising silicon and tungsten.

139. (Previously Presented) A device according to claim 134 further comprising a first interlayer insulating film over said semiconductor layer and said gate electrode, said first interlayer insulating film comprising inorganic material; a second interlayer

insulating film on said first interlayer insulating film, said second interlayer insulating film comprising organic resin; and a pixel electrode on said second interlayer insulating film.

140. (Currently Amended) A semiconductor device comprising:

a pixel portion formed over [[an]] a substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween, wherein said channel region comprises semi-amorphous silicon; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,

wherein said semiconductor layer has at least one region including carbon and overlapping both a portion of said channel region and a portion of said source and drain regions at a concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including carbon is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

141. (Previously Presented) A device according to claim 140 wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

142.-143. (Canceled)

144. (Previously Presented) A device according to claim 140 wherein said gate electrode comprises one selected from the group consisting of a silicon film containing

phosphorus, a multilayer film comprising silicon and molybdenum, and a multilayer film comprising silicon and tungsten.

145. (Previously Presented) A device according to claim 140 further comprising a first interlayer insulating film over said semiconductor layer and said gate electrode, said first interlayer insulating film comprising inorganic material; a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising organic resin; and a pixel electrode on said second interlayer insulating film.

146. (Currently Amended) A semiconductor device comprising:

a pixel portion formed over [[an]] a substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween, wherein said channel region comprises semi-amorphous silicon; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including nitrogen and overlapping both a portion of said channel region and a portion of said source and drain regions at a concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including nitrogen is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

147. (Previously Presented) A device according to claim 146 wherein said channel region contains boron at a concentration of from 1×10^{15} to 5×10^{17} atoms/cm^3.

148.-149. (Canceled)

150. (Previously Presented) A device according to claim 146 wherein said gate electrode comprises one selected from the group consisting of a silicon film containing phosphorus, a multilayer film comprising silicon and molybdenum, and a multilayer film comprising silicon and tungsten.

151. (Previously Presented) A device according to claim 146 wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

152. (Currently Amended) A semiconductor device comprising:

a pixel portion formed over [[an]] a substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween, wherein said channel region comprises semi-amorphous silicon; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including oxygen and overlapping both a portion of said channel region and a portion of said source and drain regions at a concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including oxygen is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

153. (Currently Amended) A device according to claim 152 wherein said channel region contains boron at a concentration of from 1×10^{15} to 5×10^{17} atoms/cm^3.

154.-155. (Canceled)

156. (Previously Presented) A device according to claim 152 wherein said gate electrode comprises one selected from the group consisting of a silicon film containing phosphorus, a multilayer film comprising silicon and molybdenum, and a multilayer film comprising silicon and tungsten.

157. (Previously Presented) A device according to claim 152, wherein said semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.